

FIG. 1

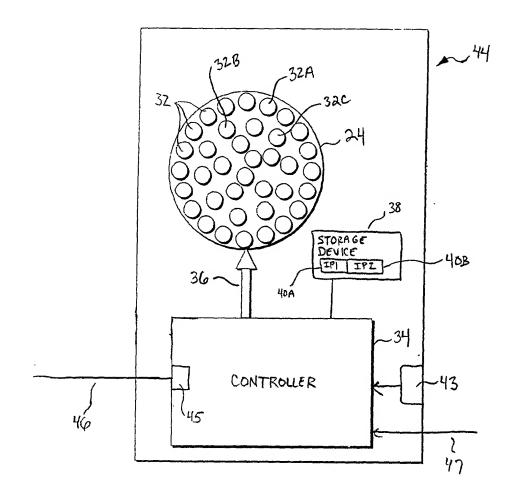


Fig. 2

manifesti (III) tidili dia

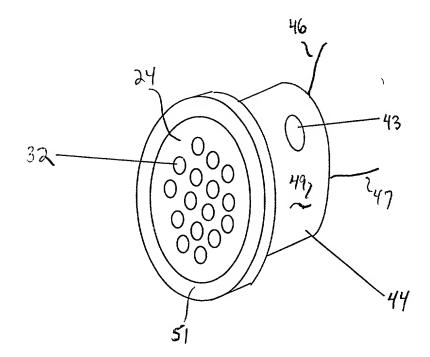
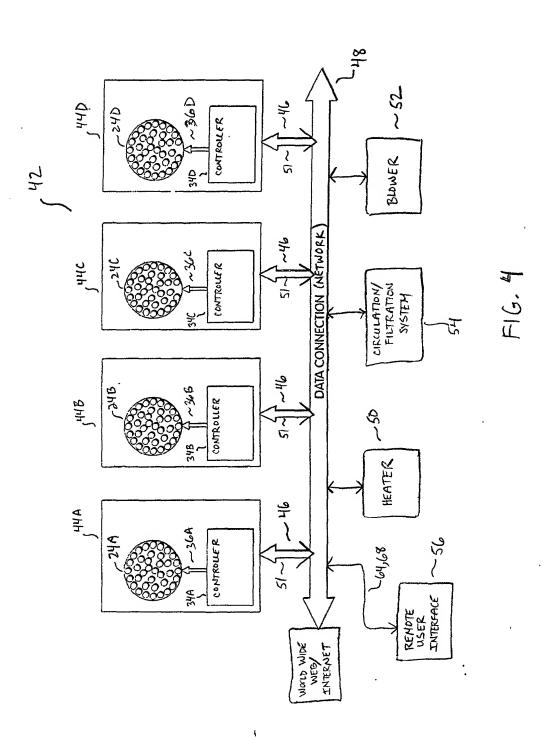
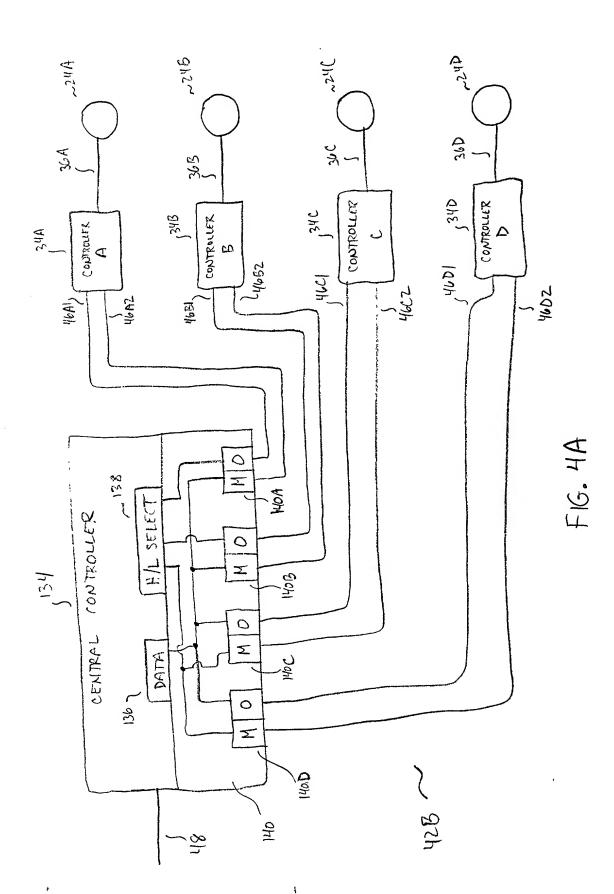


FIG.3



 λ



	The desired about the control of the		
	CONTROWER	MODE (M)	OPTION (O)
١	A	DATA	LOGIC HIGH
	В	DATA	LOGIC LOW
	0	LOGIC MGH	DATA
	D	LOGIC LOW	DATA

FIG. 4B

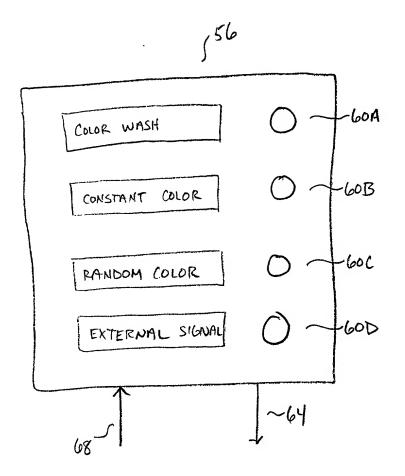


FIG. 5

AND THE RESERVE OF THE PROPERTY.

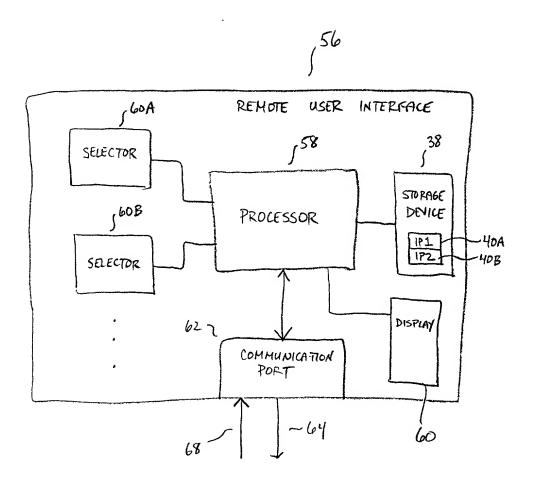


FIG. 6

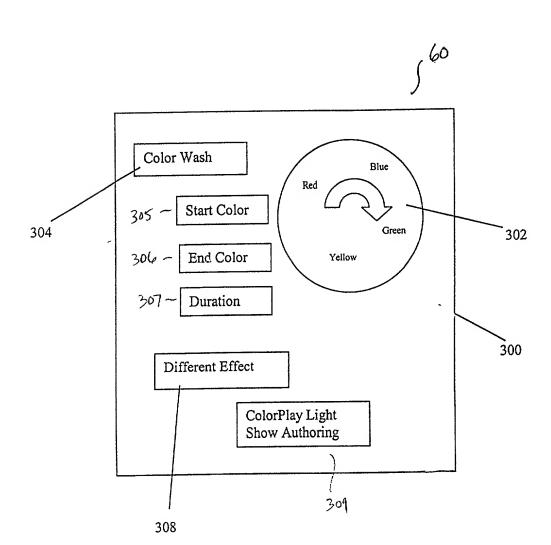


FIG. 7

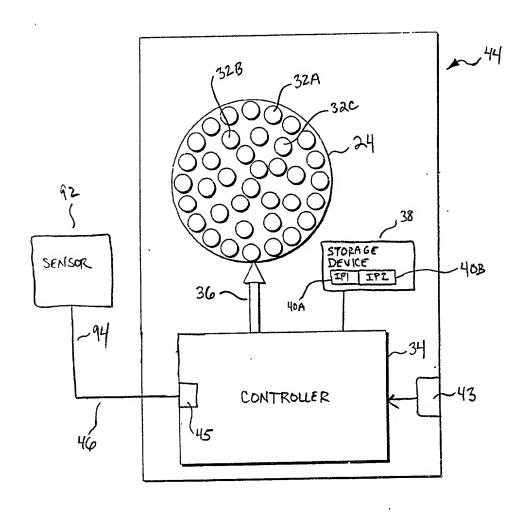
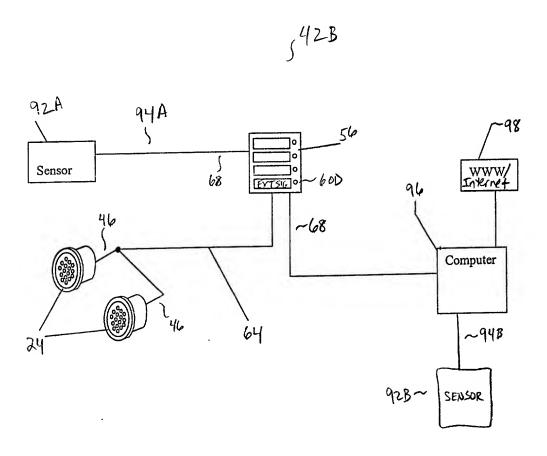


Fig. 8



F16.9

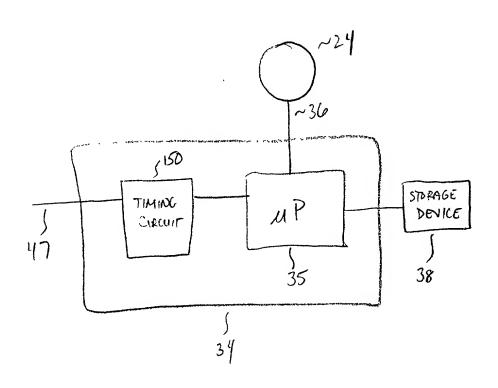


FIG. 10

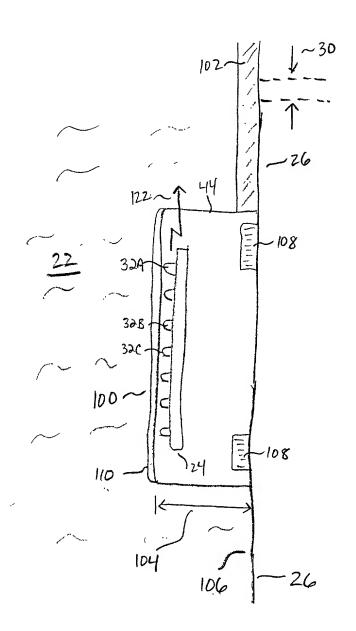
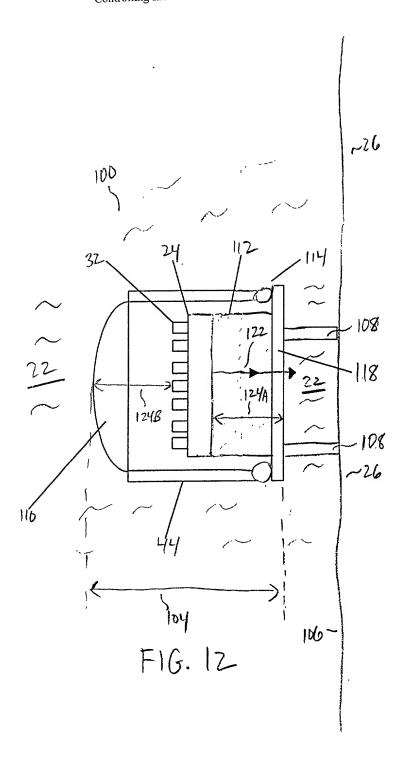


FIG. 11



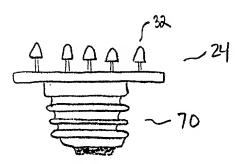


FIG 13

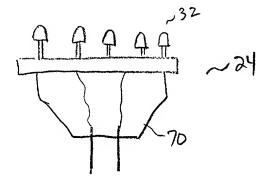


FIG. 14

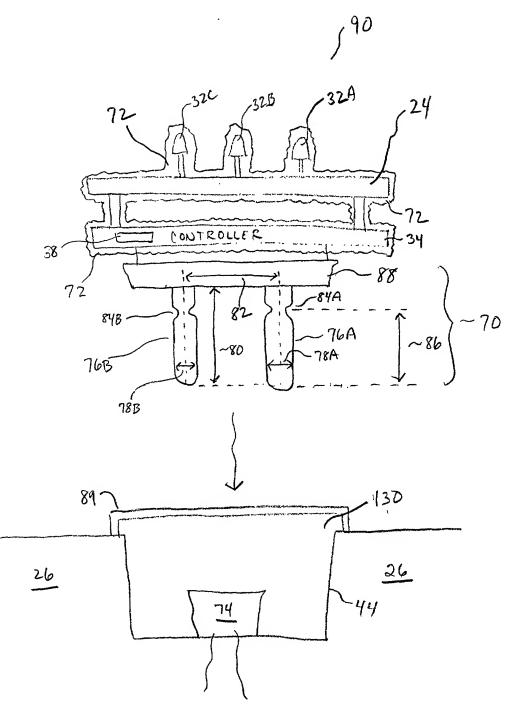
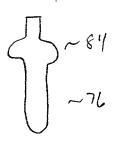


FIG. 15



F16. 16 A

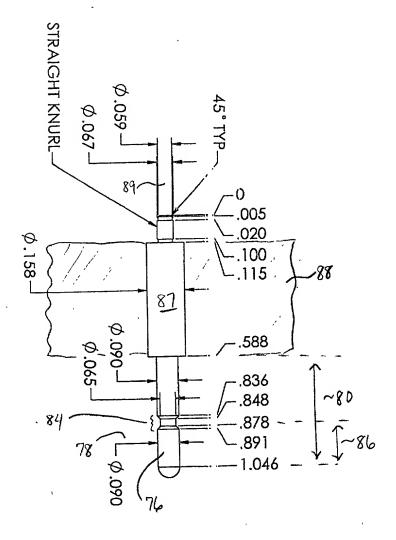
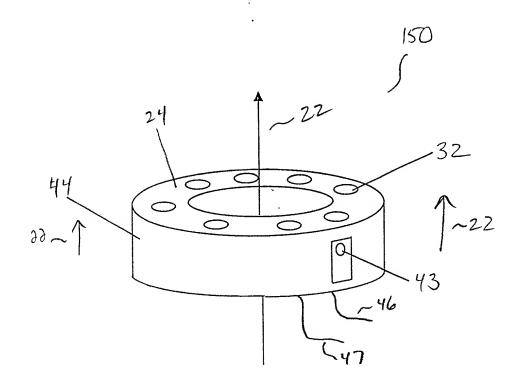
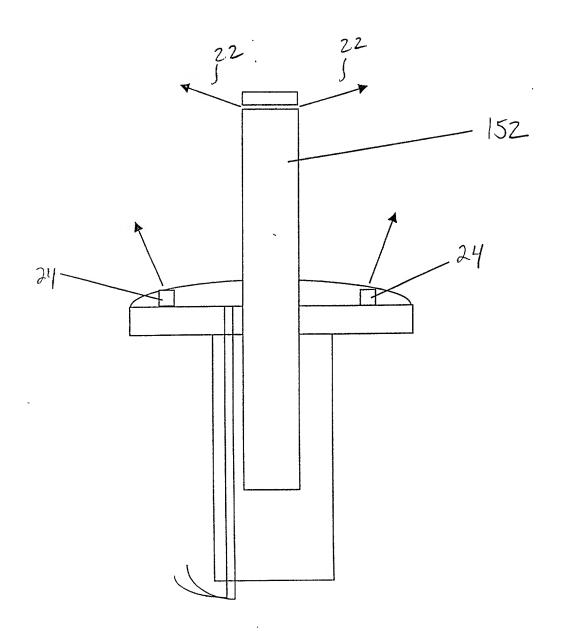


FIG. 16B

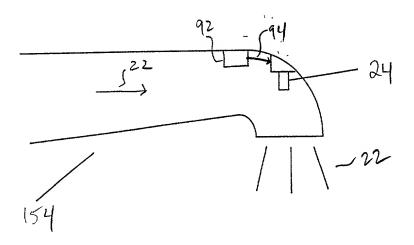


F16. 17

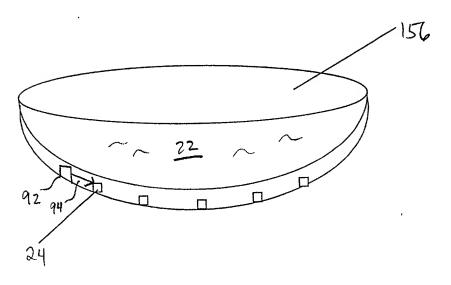


F16.18

i



F16. 19



F16.20